SGS-THOMSON MICROELECTRONICS

M108
M208

SINGLE CHIP ORGAN (SOLO + ACCOMPANIMENT)

- SIMPLE KEY SWITCH REQUIREMENTS FOR 61 KEYS, IN A MATRIX OF 12 x 6
- LOW TIME REQUIRED FOR SCANNING CYCLE OF 576 μsec.
- ACCEPTANCE OF ALL KEYS PRESSED
- TWO KEYBOARD FORMATS: 61 KEYS (SOLO) OR 24 + 37 (M108), 17 + 44 (M208) KEYS (ACC. + SOLO) WITH POSSIBILITY OF AUTOMATIC CHORDS OF THE "ACCOMPANIMENT" SECTION TOP OCTAVE SYNTHESIZER INCORPORATED FOR GENERATION OF 3 "FOOTAGES"
- MORE THAN ONE CHIP CAN BE EMPLOYED WITH SYNCHRONIZATION THROUGH THE RESET INPUT
- SEPARATED ANALOG OUTPUTS (FOR EACH FOOT) FOR "SOLO", "ACC" AND "BASS" SECTIONS (SQUARE WAVE 50% D.C.) WITH AVERAGE VALUE CONSTANT
- INTERNAL ANTI-BOUNCE CIRCUITS
- KEY DOWN AND TRIGGER OUTPUTS FOR "SOLO", "ACC." AND "BASS" SECTIONS
- SUSTAIN FOR THE LAST KEYS RELEASED IN THE "SOLO" SECTION
- CHOICE OF OPERATING MODE IN "ACC." SECTION
  - MANUAL, WITH OR WITHOUT MEMORIZATION OF THE SELECTED KEYS (FREE CHORDS WITH ALTERNATE BASS)
  - AUTOMATIC, WITH OR WITHOUT MEMORIZATION OF THE SELECTED KEY (PRIORITY TO THE LEFT FOR AUTOMATIC CHORDS AND BASS ARPEGGIO)
- MULTIPLE CHOICE POSSIBILITY ON THE CHORDS IN AUTOMATIC MODE
  - MAJOR OR MINOR THIRD
  - WITH OR WITHOUT SEVENTH
- LOW DISSIPATION OF $\leqslant$ 600 mW
- STANDARDS SINGLE SUPPLY OF +12V ± 5%
- INPUTS PROTECTED FROM ELECTROSTATIC DISCHARGES

The M108 and M208 are realized on a single monolithic chip using N-channel silicon gate technology.
They are available in a 40 lead dual in-line plastic package.

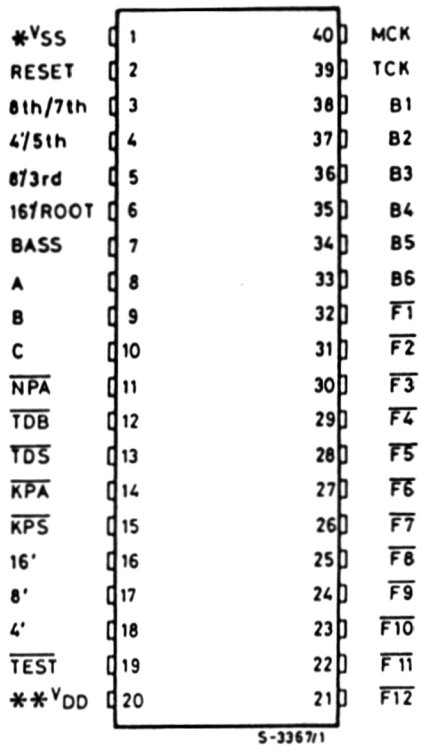
DIP-40 Plastic

ORDERING NUMBERS: M 108 B1
M 208 B1

ABSOLUTE MAXIMUM RATINGS

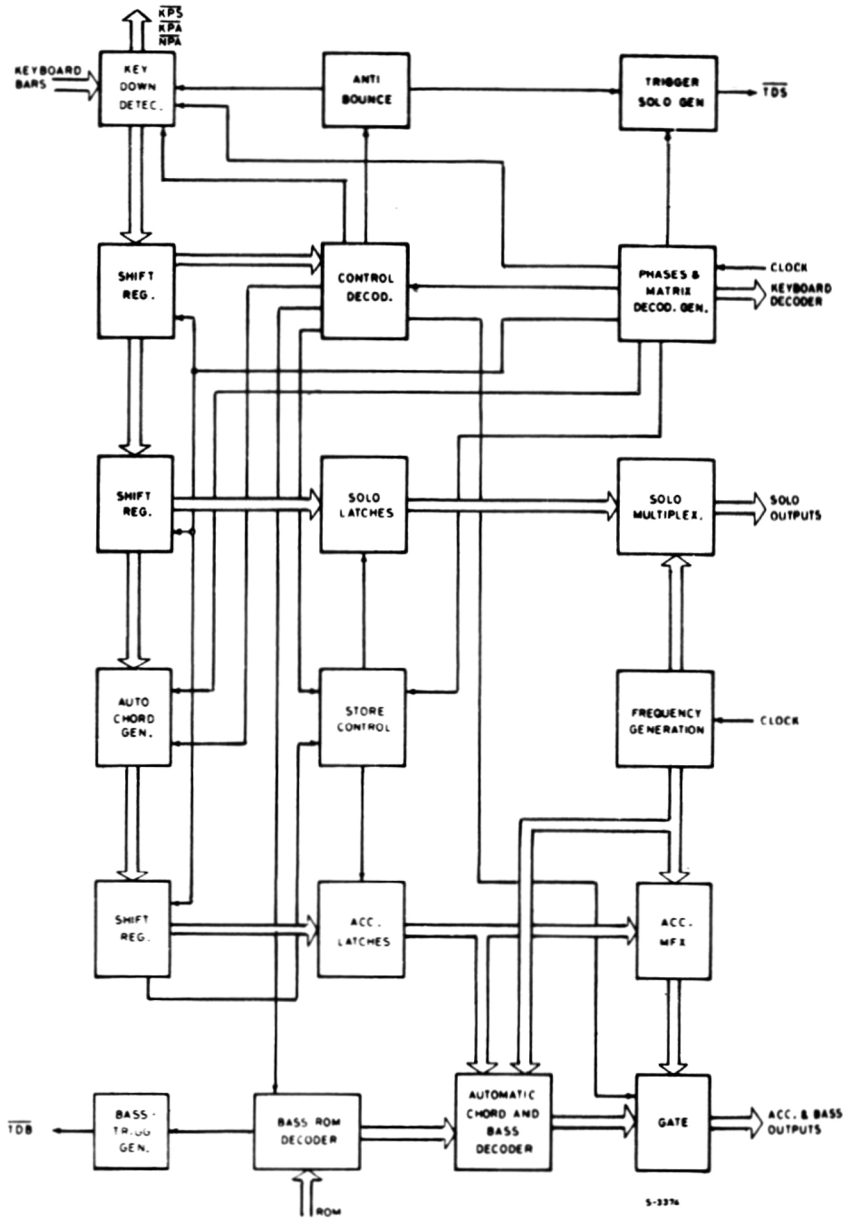
V_{DD}	Source supply voltage	-0.3 to +20	V
V_i	Input voltage	-0.3 to +20	V
I_o	Output current (at any pin)	3	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 50	°C

PIN CONNECTIONS



* V_{SS} is the lowest supply voltage
** V_{DD} is the highest supply voltage

BLOCK DIAGRAM



GENERAL CHARACTERISTICS

The caracteristics of the M208 are similar to those of the M108; the only difference is the keyboard split, which is 24+37 for the M108 and 17+44 for the M208 when used in "accompaniment + solo" mode.

The circuit comprises:

a) 2 pins for clock input: one for the matrix scanning, the other for the incorporated T.O.S.; by connecting both the clock inputs to the same matrix scanning clock (1000.12 KHz), the three "footages" generated are 16', 8' and 4'.

b) 6 inputs from the octave bars (keyboard and control scanning).

c) 3 multiplexed data inputs for addressing the bass selection. These inputs normally come from the outputs of an external memory (negative or positive logic with control inside the chip)

d) 8 signal outputs divided by section: 3 for the "SOLO" section (16', 8', 4'), 4 for the "ACC." section (16' or root, 8' or 3rd, 4' or 5th, 8th/7th according to operating mode), 1 for the bass

e) 12 outputs for the matrix scanning

f) 5 "trigger" and "key down" outputs: $\overline{KPS}$ (key pressed "SOLO"), $\overline{TDS}$ (trigger decay "SOLO"), $\overline{KPA}$ (key pressed "ACC."), $\overline{NPA}$ (pitch present in "ACC." outputs), $\overline{TDB}$ (trigger decay "BASS") respectively. These outputs, in conjunction with an external time constant, allow the formation of the envelope of the sustain and percussion effects. The duration of the trigger pulses is $\cong$ 9 msec.

g) 1 input (reset) to synchronize the device or more than one device (with the same keyboard scanning and using a single contact per key).
The reset action, provided by an external circuit, is of the "POWER ON RESET" (high active) type and its duration must be $\cong$ 0.5 msec.

h) 1 $\overline{TEST}$ pin (in use it must be connected to V_{DD})

i) 2 supply pins.

MATRIX ORGANIZATION (Keyboard and controls)

M108/208 Matrix outputs	M108/208 Octave bar inputs					
	B_1	B_2	B_3	B_4	B_5	B_6
$\overline{F_1}$	C_1	C_2	C_3	C_4	C_5	C_6
$\overline{F_2}$	C_1#	C_2#	C_3#	C_4#	C_5#	7th OFF/7th ON
$\overline{F_3}$	D_1	D_2	D_3	D_4	D_5	3rd+/3rd-
$\overline{F_4}$	D_1#	D_2#	D_3#	D_4#	D_5#	Sust. OFF/Sust. ON
$\overline{F_5}$	E_1	E_2	E_3	E_4	E_5	$\overline{Latch}$/Latch
$\overline{F_6}$	F_1	F_2	F_3	F_4	F_5	Man/Auto
$\overline{F_7}$	F_1#	F_2#	F_3#	F_4#	F_5#	61/24 + 37 (17 + 44)
$\overline{F_8}$	G_1	G_2	G_3	G_4	G_5	Antibounce ON/Antibounce OFF
$\overline{F_9}$	G_1#	G_2#	G_3#	G_4#	G_5#	ROM Low/ROM High
$\overline{F_{10}}$	A_1	A_2	A_3	A_4	A_5	-------
$\overline{F_{11}}$	A_1#	A_2#	A_3#	A_4#	A_5#	-------
$\overline{F_{12}}$	B_1	B_2	B_3	B_4	B_5	-------

C_1 is the first key on the left, C_6 is the last key on the right of the keyboard.

The main feature of this chip is the possibility of formating the keyboard either with 61 keys (only "SOLO" without automatism) or separating it into two sections ("ACCOMPANIMENT + SOLO") with the possibility of chord and bass automatic in the first section.

FEATURES

a) The "61/24 + 37" (17 + 44) control chooses the keyboard operating mode, i.e. the whole keyboard dedicated to "SOLO" or 24 (17) keys dedicated to "ACCOMPANIMENT" and 37 (44) to "SOLO".

b) The "Man/Auto" control, which operates only in case of "ACC.+ SOLO", chooses the manual or the automatic accompaniment.

c) The "Sust OFF/Sust ON" allows the storage of the "SOLO" section and handles the whole keyboard or 37 (44) keys depending on the operating mode.

d) The "$\overline{\text{Latch}}$/Latch" similarly allows the storage of the "ACC." section and operates in "ACC.+ SOLO" only.

e) The "3rd+/3rd-" which operates only in case of "ACC.+ SOLO" and "AUTOMATIC", changes the automatic chord generated from major to minor or viceversa.

f) The "7th OFF/7th ON" adds the seventh to the automatic chord generated.

g) The "Antibounce ON/Antibounce OFF" disables the antibounce circuit which is usually enabled.

h) The "ROM Low/ROM High" selects between ROMs with return to "1" (Low active) or with return to "0" (High active). Usually the chip is enabled for ROMs with return to "1" (Low active).

"SOLO" Operation

In this case the chip recognizes the whole keyboard as "SOLO" and does not read the controls which concern the "ACC.+ SOLO" operation.
The chip identifies all the keys pressed and transfers to the outputs of each section (ACC. and SOLO) the analog sum of corresponding pitches.
The outputs are current generators with average value constant, therefore it is sufficient to connect the pins to one load and send the signals on to the filters.
In the case of "Sustain OFF" each new key pressed or released is accepted or deleted in a time $\leqslant 576\ \mu$sec.
In the case of "Sustain ON" the chip has a different operation according to whether the new key (keys) is pressed or released: each new key pressed is always accepted in a time $\leqslant 576\ \mu$sec., whereas each key released is deleted with a delay of 73 msec. and only if there are still keys pressed.
In fact, if after the 73 msec. there are no keys pressed, the last key (or keys) released remains stored until new keys are pressed.
In this mode it is possible to have Sustain, with external envelope shaping, for the last keys (or key) released.
The pitch envelope is controlled by a D.C. signal $\overline{\text{KPS}}$ (any key pressed) and there is also an A.C. signal $\overline{\text{TDS}}$ (trigger decay "SOLO") which provides a pulse whenever a key is pressed.
An appropriate antibounce circuit, inside the chip, solves the problems associated with the keyboard contacts.

"SOLO + ACCOMPANIMENT" Operation

In this case the chip identifies the "ACCOMPANIMENT" on the first 24 (17) keys on the left, and the "SOLO" on the remaining 37 (44) keys and reads all the controls which concern the "ACC." section.
The "SOLO" function is identical to "61 keys" mode, but for the "ACC." section there are two possibilities:

A) **MANUAL**
The chip identifies which keys are pressed in the "ACC." section, and transfers to the "ACC." outputs the analog sum of the corresponding pitches.
The "ACC." section is fully independent of the "SOLO" section and the signals (if there is no "LATCH") remain at the output only while the keys are pressed even if there is "SUSTAIN ON".

The "BASS" section gives at the bass output an alternating bass between the first on the left and the first on the right of the keys pressed in the "ACC." section; the pitch switching timing is dependent on an external ROM (3 bits).
The "LATCH" control stores the last keys released and the output signals, including the bass output, remain until new keys are pressed.
The $\overline{TDB}$ (trigger decay "BASS") output gives a pulse corresponding to every output change; there are also two D.C. signals, $\overline{KPA}$ (any key pressed accompaniment) and $\overline{NPA}$ (pitches in output accompaniment) relative only to the "ACC." section.
The first of these signals (analogous to $\overline{KPS}$) concerns the keyboard and does not consider the "LATCH" condition.
The second on the contrary concerns the "ACC." output and considers the "LATCH" condition.

B) AUTOMATIC

The chip recognizes in the "ACC." section only the first on the left of the keys pressed and, according to the setting of the following controls, produces a major or minor chord with or without seventh only the 4' footage but with separated outputs for root, third, fifth and eighth (or seventh if the chord is with seventh).
The bass section gives the bass arpeggio among root, third, fourth, fifth, sixth, seventh and eighth with pitch switching dependent on an external ROM (3 bits).
In automatic mode the two octaves of the "ACC." section inside the chip are connected in parallel both for the chord and for the bass; therefore by pressing anyone of the two keys of the same note the chip generates the same chord.
The "LATCH" control stores the major chord and the bass pitches (until new keys are pressed); the modification of the chord stored (from major to minor, addition of seventh) is always possible by operating the proper controls: by releasing these controls the chord becomes major again.
It is possible to delete the stored pitches both is manual and in "AUTOMATIC" mode by a $\overline{Latch}$ control signal.
Once again there are $\overline{KPA}$, $\overline{NPA}$, and $\overline{TDB}$ information; however the $\overline{TDB}$ pulse, which normally appears at each arrival of the ROM codes, does not appear if there are no pitches in the "ACC." (and bass) outputs or, in the case of alternate bass (in manual mode) if the codes indicate conditions of indifference.

RECOMMENDED OPERATING CONDITIONS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{SS}	Lowest supply voltage		0		0	V
V_{DD}	Highest supply voltage		11.4	12	12.6	V

BASS TRUTH TABLES

LOW ACTIVE

External Memory Code			Bass Arpeggio Output (Automatic mode)	Alternate Bass Output (Manual mode)
C	B	A		
1	1	1	No change	No change
1	1	0	Root	1st on the left
1	0	1	3rd	– – –
1	0	0	4th	– – –
0	1	1	5th	1st on the right
0	1	0	6th	– – –
0	0	1	7th	– – –
0	0	0	8th	– – –

HIGH ACTIVE

External Memory Code			Bass Arpeggio Output (Automatic mode)	Alternate Bass Output (Manual mode)
C	B	A		
0	0	0	No change	No change
0	0	1	Root	1st on the left
0	1	0	3rd	– – –
0	1	1	4th	– – –
1	0	0	5th	1st on the right
1	0	1	6th	– – –
1	1	0	7th	– – –
1	1	1	8th	– – –

STATIC ELECTRICAL CHARACTERISTICS (Positive Logic, V_{DD} = +12V ± 5%, V_{SS} = 0V, T_{amb} = 0 to 70°C unless otherwise specified)

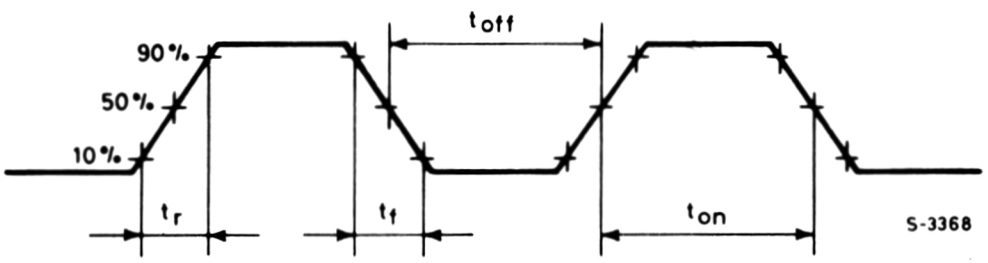
Parameter		Test conditions	Min.	Typ.	Max.	Unit
INPUT SIGNALS						
V_{IH}	Input high voltage	Note 1	V_{DD}-1		V_{DD}	V
		Note 2	4		18	V
		Note 3	V_{DD}-2		V_{DD}	V
V_{IL}	Input low voltage	Note 1	V_{SS}		V_{SS}+1	V
		Note 2	V_{SS}		V_{SS}+0.6	V
		Note 3	V_{SS}		V_{SS}+2	V
I_{LI}	Input leakage current	V_I= +12.6V T_{amb}= 25°C			10	µA
LOGIC SIGNAL OUTPUTS						
R_{ON}	Output resistance with respect to V_{SS}			300	500	Ω
R_{ON}	Output resistance with respect to V_{DD}	V_{OUT}= V_{DD}-1 (driver off)		15	25	kΩ
V_{OH}	Output high voltage		V_{DD}-0.4		V_{DD}	V
V_{OL}	Output low voltage			V_{SS}+0.2	V_{SS}+0.4	V
POWER DISSIPATION						
I_{DD}	Supply current	T_{amb}= 25°C		30	45	mA
ANALOG SIGNAL OUTPUTS (the external load must be connected to $V_{DD}/2$)						
I_{OH}	Output current with respect to $V_{DD}/2$	Outputs loaded with 1 KΩ resistor versus $V_{DD}/2$	8	20		µA
I_{OL}	Output current with respect to V_{SS}	Outputs loaded with 1 KΩ resistor versus $V_{DD}/2$	-8	-20		µA

Note 1 : Refers only to the clock inputs.
Note 2 : Refers only to the inputs from the external memory.
Note 3 : Refers only to the reset input.

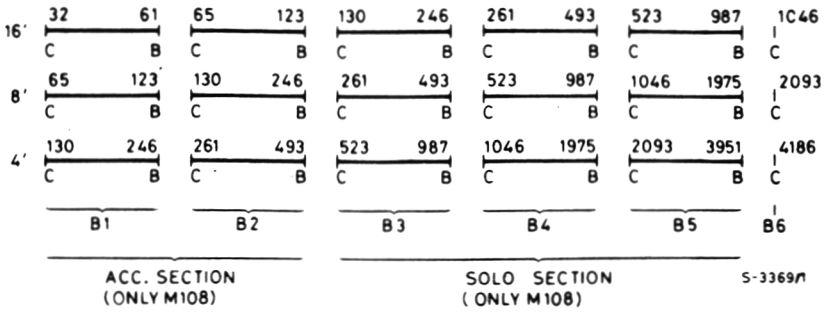
DYNAMIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
MASTER CLOCK INPUT						
f_i	Input clock frequency		800	1000.12		KHz
t_r, t_f	Input clock rise and fall time 10% to 90%	1000.12 KHz			40	ns
t_{on}, t_{off}	Input clock ON and OFF times	1000 KHz		500		ns
T.O.S. CLOCK INPUT						
f_i	Input clock frequency		100	1000.12	2500	KHz
t_r, t_f	Input clock rise and fall times 10% to 90%	1000.12 KHz			40	ns
t_{on}, t_{off}	Input clock ON and OFF times	2000 KHz		250		ns
$\overline{TDS}$ and $\overline{TDB}$ OUTPUTS						
t_{on}	Pulse duration	1000 KHz		9.216		ms
t_r, t_f	Outputs rise and fall times 10% to 90%	1000 KHz		100		ns

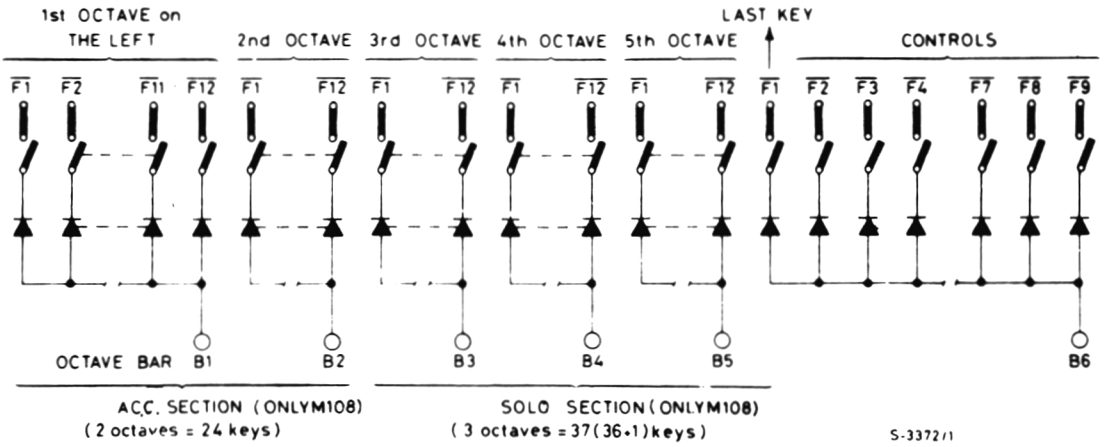
INPUT CLOCK WAVEFORM



FREQUENCY RANGE OF EACH OCTAVE (16', 8', 4' footages)

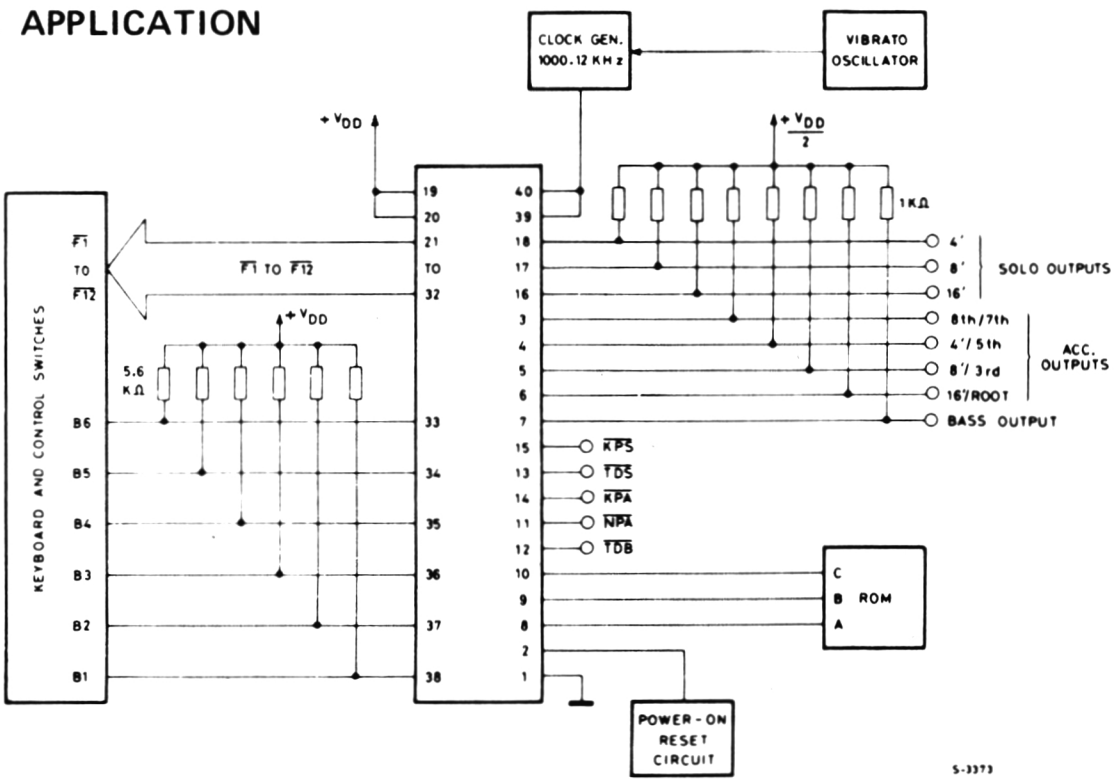


CONNECTION OF THE KEYBOARD AND CONTROL SWITCHES

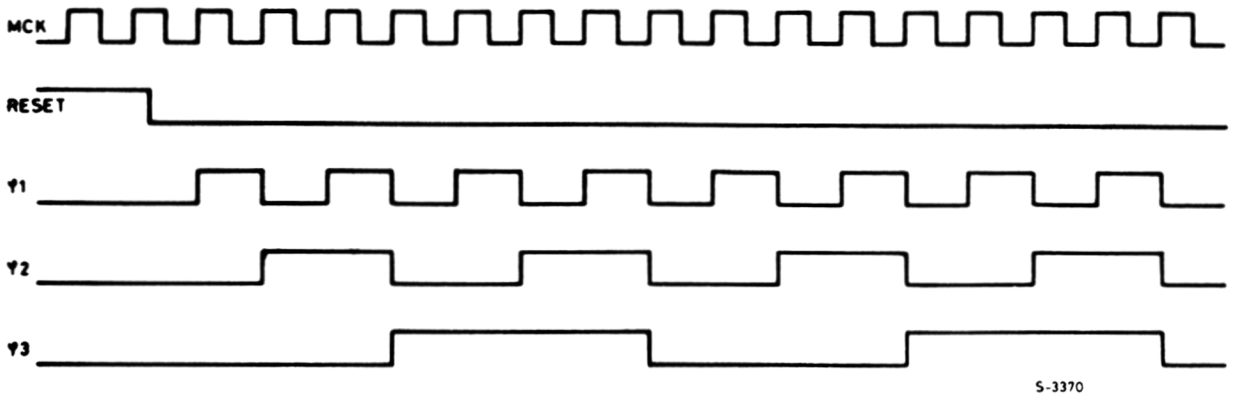


Note: The switch "OPEN" corresponds to "KEY NOT PRESSED" or "CONTROL IN THE FIRST CONDITION" (see the drawing "MATRIX ORGANIZATION").

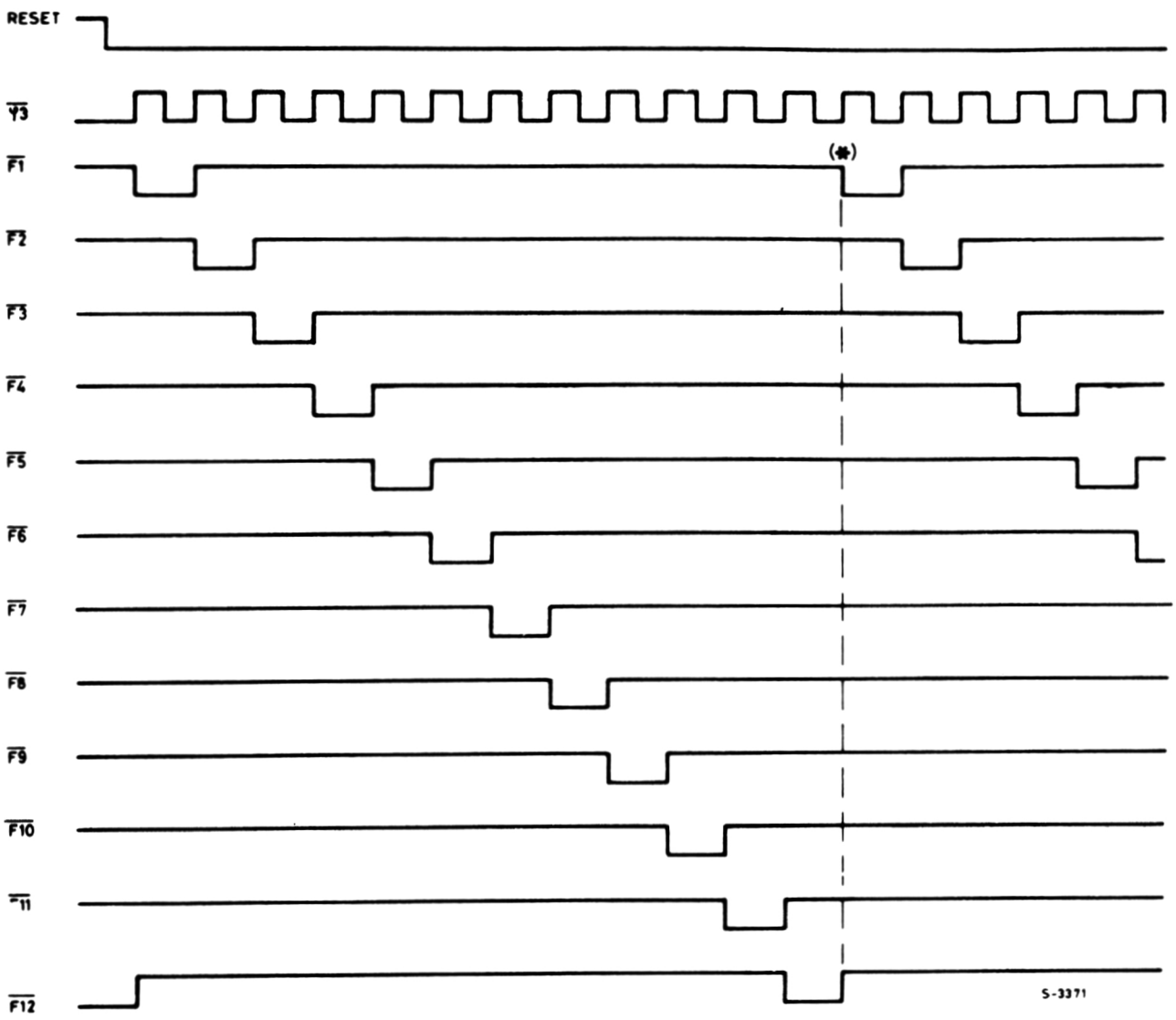
TYPICAL APPLICATION



TIMING DIAGRAMS



Note: MCK is the master clock input (matrix scanning), $\varphi 1$, $\varphi 2$, $\varphi 3$ are internal phases to generate $\overline{F1} \div \overline{F12}$.



Note: The matrix scanning starts (after the power on reset) at the second arrival in output of $\overline{F1}$ (*) from B1 to B6 i
continuous sequence.