

Z0103/07/09 series

Triacs

Rev. 02 — 12 September 2002

Product data

1. Product profile

1.1 Description

Passivated triacs in conventional and surface mounting packages. Intended for use in applications requiring high bidirectional transient and blocking voltage capability. Available in a range of gate current sensitivities for optimum performance.

Product availability:

Z0103MA; Z0103NA; Z0107MA; Z0107NA; Z0109MA; Z0109NA in SOT54B
Z0103MN; Z0103NN; Z0107MN; Z0107NN; Z0109MN; Z0109NN in SOT223.

1.2 Features

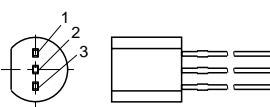

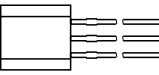

- Blocking voltage to 800 V (NA and NN types)
- 1 A on-state RMS current.

1.3 Applications

- Home appliances
- Fan controllers
- Small motor control
- Small loads in industrial process control.

2. Pinning information

Table 1: Pinning - SOT54B (TO-92), SOT223, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	terminal 2 (T2)		
2	gate (G)		
3	terminal 1 (T1)		
1	terminal 1 (T1)		
2	terminal 2 (T2)		
3	gate (G)		
4	terminal 2 (T2)		

SOT54B (TO-92) **SOT223**



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3. Ordering information

3.1 Ordering options

Table 2: Ordering information

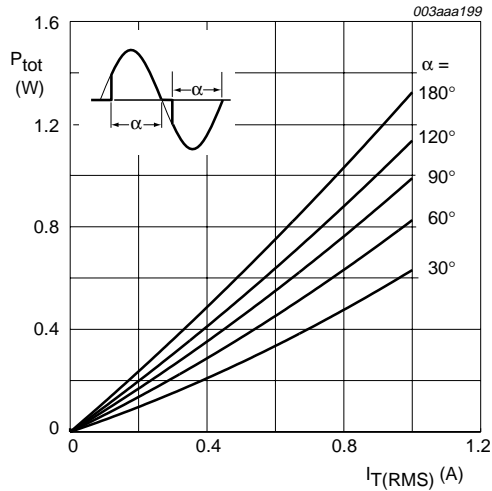
Part Number	Voltage (V _{DRM})	Gate Sensitivity (I _{GT})	Package
Z0103MA	600 V	3 mA	SOT54B (TO-92)
Z0103NA	800 V	3 mA	SOT54B (TO-92)
Z0107MA	600 V	5 mA	SOT54B (TO-92)
Z0107NA	800 V	5 mA	SOT54B (TO-92)
Z0109MA	600 V	10 mA	SOT54B (TO-92)
Z0109NA	800 V	10 mA	SOT54B (TO-92)
Z0103MN	600 V	3 mA	SOT223
Z0103NN	800 V	3 mA	SOT223
Z0107MN	600 V	5 mA	SOT223
Z0107NN	800 V	5 mA	SOT223
Z0109MN	600 V	10 mA	SOT223
Z0109NN	800 V	10 mA	SOT223

4. Limiting values

Table 3: Limiting values

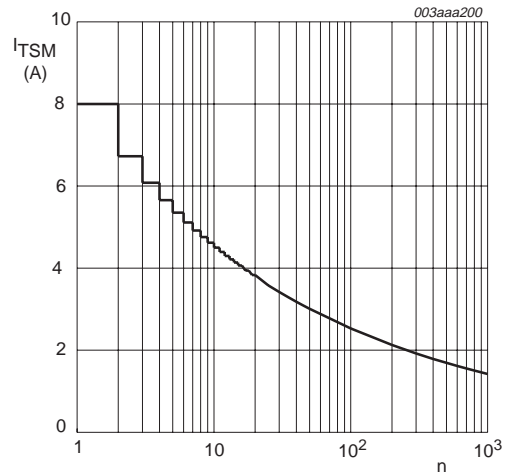
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DRM}	repetitive peak off-state voltage	25 °C ≤ T _j ≤ 125 °C			
	Z0103/07/09MA; Z0103/07/09MN		-	600	V
	Z0103/07/09NA; Z0103/07/09NN		-	800	V
V _{RPM}	repetitive peak reverse voltage	25 °C ≤ T _j ≤ 125 °C			
	Z0103/07/09MA; Z0103/07/09MN		-	600	V
	Z0103/07/09NA; Z0103/07/09NN		-	800	V
I _{TSM}	non-repetitive peak on-state current	full sine wave; T _j = 25 °C prior to surge; Figure 2 and Figure 3			
		t = 20 ms	-	8	A
		t = 16.7 ms	-	8.5	A
I _{T(RMS)}	RMS on-state current	all conduction angles; Figure 4			
	SOT223	T _{sp} = 90 °C	-	1	A
	SOT54B (TO-92)	T _{lead} = 50 °C	-	1	A
I ² t	I ² t for fusing	t = 10 ms	-	0.35	A ² s
di _T /dt	rate of rise of on-state current	I _{TM} = 1.0 A; I _G = 2 × I _{GT} ; di _G /dt = 100 mA/μs	-	20	A/μs
I _{GM}	peak gate current	t _p = 20 μs	-	1.0	A
P _{GM}	peak gate power		-	2.0	W
P _{G(AV)}	average gate power	over any 20 ms period	-	0.1	W
T _{stg}	storage temperature		-40	+150	°C
T _j	junction temperature		-40	+125	°C



α = conduction angle

Fig 1. Maximum on-state power dissipation as a function of RMS on-state current; typical values.



n = number of cycles at $f = 50$ Hz

Fig 2. Maximum permissible non-repetitive peak on-state current as a function of number of cycles for sinusoidal currents; typical values.

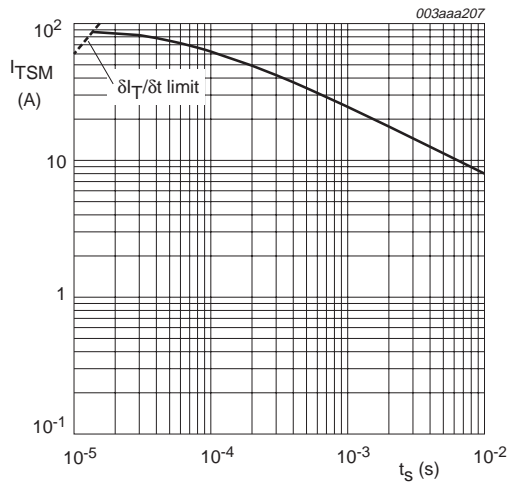


Fig 3. Maximum permissible non-repetitive peak on-state current as a function of surge duration for sinusoidal currents; typical values.

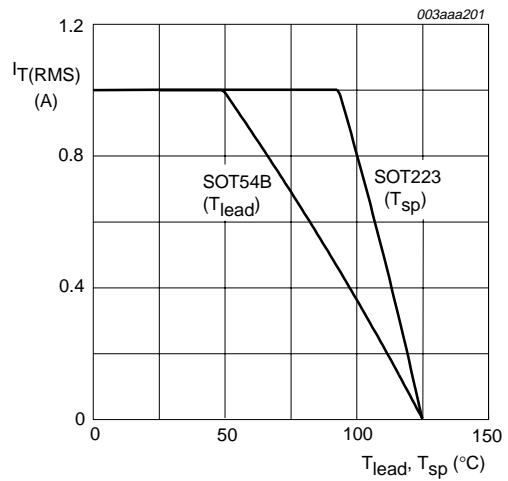


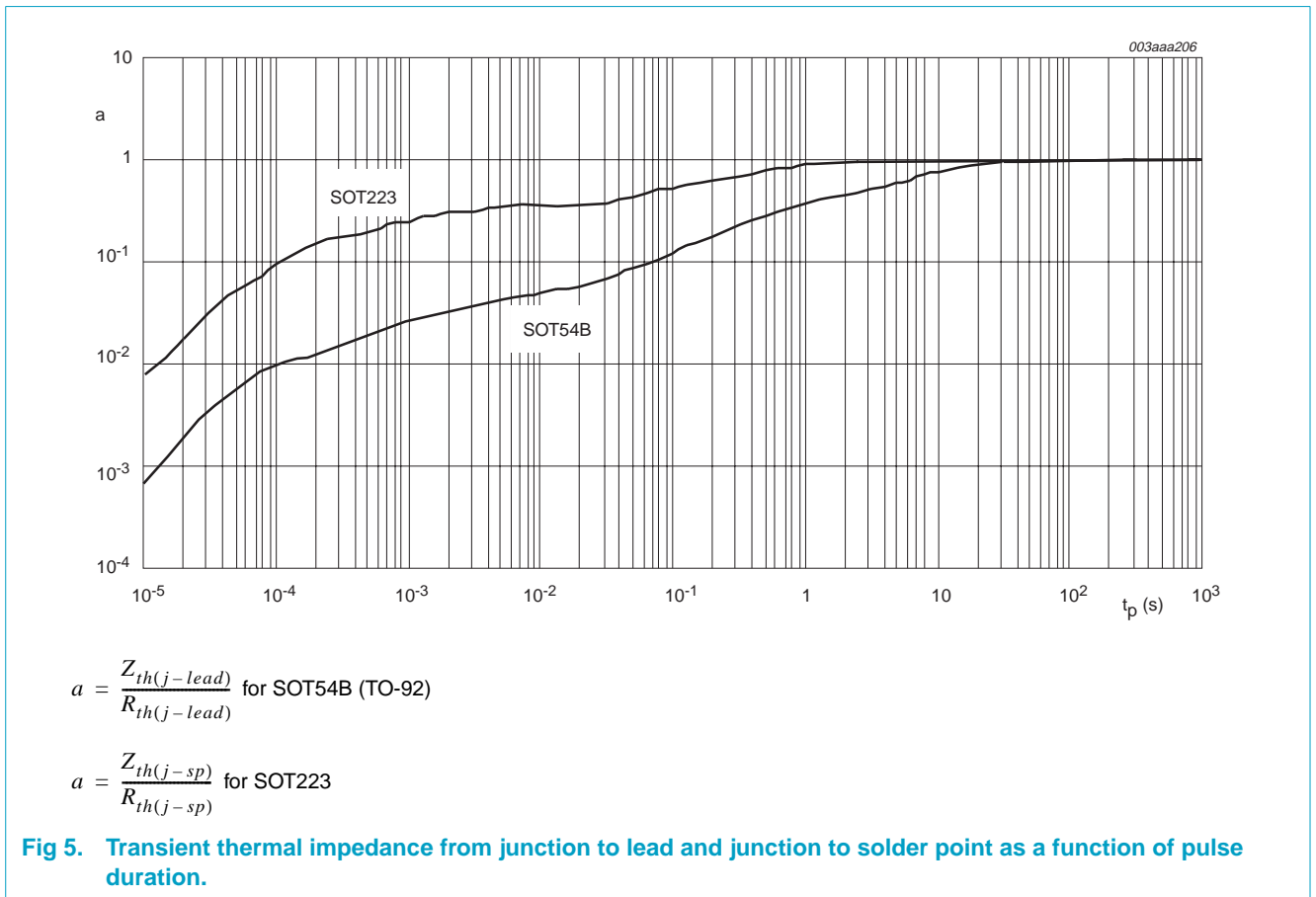
Fig 4. Maximum permissible RMS on-state current as a function of lead temperature and solder point temperature; typical values.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point for SOT223	Figure 5	-	-	25	K/W
$R_{th(j-lead)}$	thermal resistance from junction to lead for SOT54B (TO-92)	Figure 5	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT223	minimum footprint; mounted on a PCB	-	60	-	K/W
	SOT54B (TO-92)	vertical in free air	-	150	-	K/W

5.1 Transient thermal impedance



6. Characteristics

Table 5: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $R_L = 30\ \Omega$; T2+ G+; T2+ G-; T2- G-; Figure 9	-	-	3	mA	
	Z0103MA/MN/NA/NN		-	-	5	mA	
	Z0107MA/MN/NA/NN		-	-	10	mA	
	Z0103MA/MN/NA/NN	$V_D = 12\text{ V}$; $R_L = 30\ \Omega$; T2- G+; Figure 9	-	-	5	mA	
	Z0107MA/MN/NA/NN		-	-	7	mA	
	Z0109MA/MN/NA/NN		-	-	10	mA	
I_L	latching current	$V_D = 12\text{ V}$; $R_L = 30\ \Omega$; T2+ G+; T2- G-; T2- G+; Figure 7	-	-	7	mA	
	Z0103MA/MN/NA/NN		-	-	10	mA	
	Z0107MA/MN/NA/NN		-	-	15	mA	
	Z0103MA/MN/NA/NN	$V_D = 12\text{ V}$; $R_L = 30\ \Omega$; T2+ G-; Figure 7	-	-	15	mA	
	Z0107MA/MN/NA/NN		-	-	20	mA	
	Z0109MA/MN/NA/NN		-	-	25	mA	
I_H	holding current	$I_T = 50\text{ mA}$; Figure 8	-	-	7	mA	
	Z0103MA/MN/NA/NN		-	-	10	mA	
	Z0109MA/MN/NA/NN		-	-	10	mA	
V_T	on-state voltage	Figure 6	-	1.3	1.6	V	
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $R_L = 30\ \Omega$; $T_j = 25\text{ °C}$; Figure 11	-	-	1.3	V	
		$V_D = V_{DRM}$; $R_L = 3.3\text{ k}\Omega$; $T_j = 125\text{ °C}$; Figure 11	0.2	-	-	V	
I_D	off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j = 125\text{ °C}$	-	-	500	μA	
Dynamic characteristics							
dV_D/dt	critical rate of rise of off-state voltage	$V_D = 0.67 V_{DRM(max)}$; $T_j = 110\text{ °C}$; exponential waveform; gate open; Figure 10	10	-	-	V/ μs	
			Z0103MA/MN/NA/NN	20	-	-	V/ μs
			Z0107MA/MN/NA/NN	50	-	-	V/ μs
dV_{com}/dt	critical rate of change of commutating voltage	$V_D = 400\text{ V}$; $I_T = 1\text{ A}$; $T_j = 110\text{ °C}$; $dI_{com}/dt = 0.44\text{ A/ms}$; gate open	0.5	-	-	V/ μs	
			Z0103MA/MN/NA/NN	1	-	-	V/ μs
			Z0107MA/MN/NA/NN	2	-	-	V/ μs
Z0109MA/MN/NA/NN							

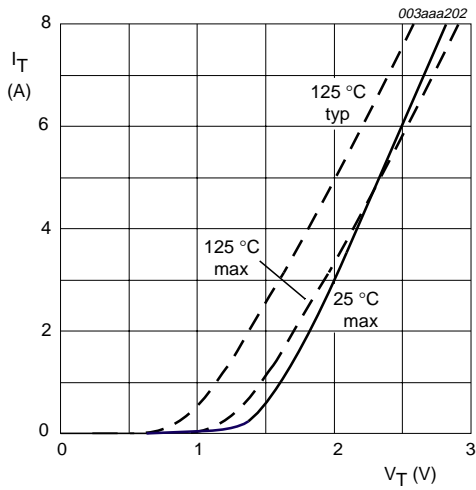
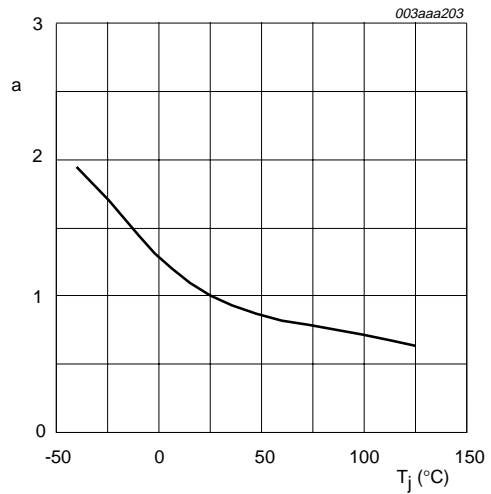
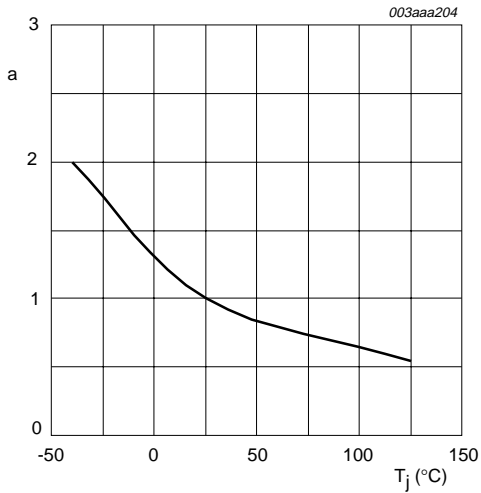


Fig 6. On-state current as a function of on-state voltage; typical and maximum values.



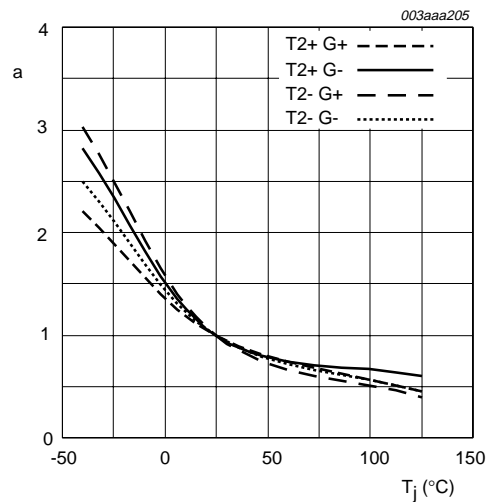
$$a = \frac{I_L}{I_{L(25^\circ\text{C})}}$$

Fig 7. Normalized latching current as a function of junction temperature; typical values.



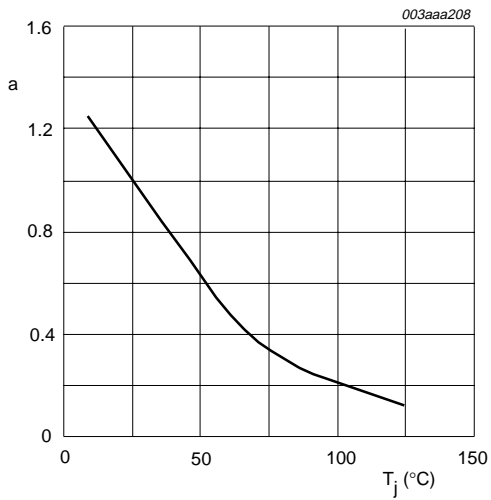
$$a = \frac{I_H}{I_{H(25^\circ\text{C})}}$$

Fig 8. Normalized holding current as a function of junction temperature; typical values.



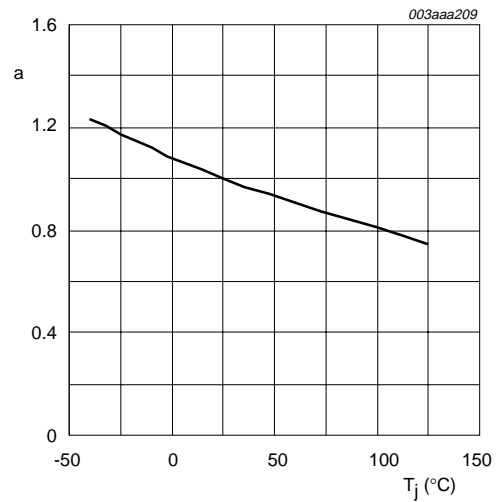
$$a = \frac{I_{GT}}{I_{GT(25^\circ\text{C})}}$$

Fig 9. Normalized gate trigger current as a function of junction temperature; typical values.



$$a = \frac{dV_D/dt}{dV_{D(25^\circ C)}/dt}$$

Fig 10. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values.



$$a = \frac{V_{GT}}{V_{GT(25^\circ C)}}$$

Fig 11. Normalized gate trigger voltage as a function of junction temperature; typical values.

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54B

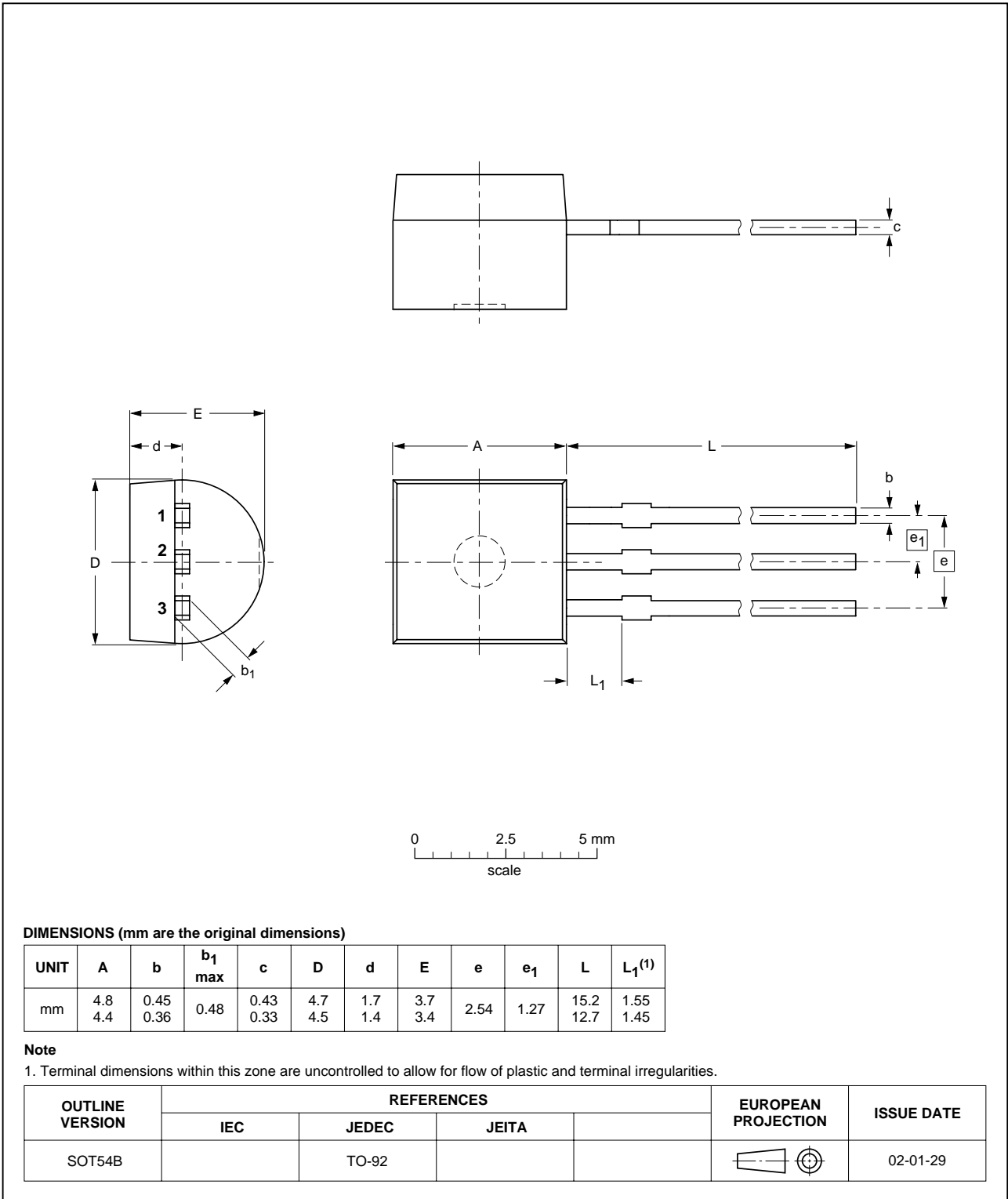


Fig 12. SOT54B (TO-92).

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223

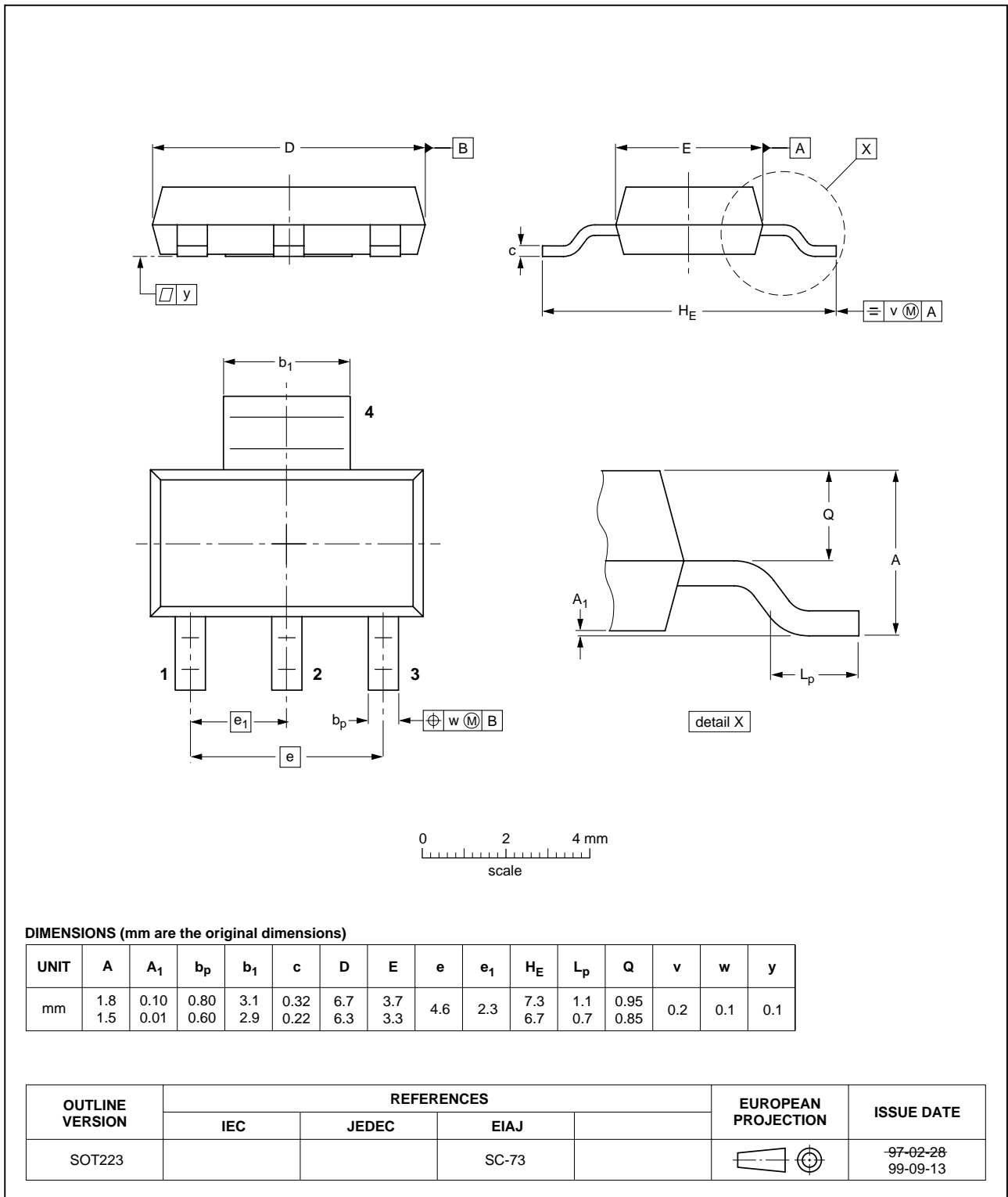


Fig 13. SOT223.

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20020912		Product data; supersedes data of 11 April 2002 Table 5 "Characteristics" Addition of dV_{com}/dt data. Correction to dV_D/dt data
01	20020411	-	Product data; initial version (9397 750 09419)

9. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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